REMARKS

Claims 1-11 are currently pending in the patent application. The Examiner has rejected Claim 11 as indefinite; Claims 1, 8, and 9 under 35 USC 102 as anticipated by Benkual; Claims 2-3 as unpatentable over Benkual in view of Burger; Claims 4-5 as unpatentable over Burger; and, Claims 6, 7, 10 and 11 as unpatentable over Burger in view of Benkual.

Applicants have amended Claim 11 to address the Examiner's concerns regarding indefiniteness due to a missing period at the end. In addition, Applicants have amended several other claims to correct grammatical errors and to more appropriately delimit the features of the claimed apparatus.

The Benkual patent is directed to a "Random-In-First-Out" (RIFO) buffer for re-ordering data in a computer system. At Col. 19, lines 1-30, Benkual details reserving specific memory locations in the RIFO memory region for specific data which is currently being operated on. Benkual does not, however, teach or suggest that a fence instruction be issued for an entire memory region. Further, Benkual does not teach any threshold other than a "full" RIFO threshold for an entire memory region (see: Col.

19, lines 58-62). Clearly, therefore, it cannot be maintained that Benkual teaches that an instruction threshold, which is not a "full" threshold, be evaluated and that a fence instruction be issued for an entire region of memory. The teachings cited from Col. 6-Col. 7 detail counters for in-order and out-of-order RIFO buffer data. Applicants respectfully assert that those teachings neither anticipate nor obviate the claimed recitation of steps and means for incrementing and decrementing a counter with outstanding instructions associated with a memory region and comparing those to a threshold.

With regard to the fence instruction claim language, the Examiner has cited the teachings from Col. 17, lines 6-40 of Benkual. The cited teachings detail determining if there is data to be written and writing that data. While a fence instruction is noted, there are no teachings of issuing a fence instruction for an entire memory region based on a threshold determination. Moreover, the aforementioned teachings from Col. 19 expressly teach that only specific sequential (i.e., "in-order") memory locations will be reserved for data. Benkual does not teach issuing a fence instruction for an entire memory region.

With regard to the language of Claims 8 and 9 regarding counters, the cited passage from Benkual Col. 17, line

63-Col. 18, lines 26 details that even if the DWASSB has changed, with a change indicating the presence of a write fence (Col. 18, lines 11-12), Benkual simply shifts the count from the out-of-order to the in-order count and still writes datum to the device (Col. 18, lines 17-24). Applicants respectfully assert that the Benkual patent effectively teaches away from the claim language, since Benkual uses counters to shift data within a memory but not to prevent data writes to that memory. In addition, the counters of Benkual are used to "count" available memory space and not to count the number of outstanding instructions. Similarly, the threshold of Benkual is a memory space threshold (i.e., FULL) whereas the claimed invention provides a threshold number of outstanding instructions.

It is well established under U. S. Patent Law that, for a reference to anticipate claim language under 35 USC 102, that reference must teach each and every claim feature. Since the Benkual patent does not teach steps or means for determining if the number of outstanding write instructions targeted to a designated region of memory is above a threshold and issuing a fence instructions such that no further instructions are issued from the processor to that region until the number of outstanding writes has fallen

below the threshold, it cannot be maintained that Benkual anticipates the invention as set forth in the independent claims, Claims 1, 8 and 9.

The additionally cited patent is the Burger patent, which provides a method and apparatus for ensuring that modifications to the control register in a computer will be observed by all subsequent instructions. Burger uses one of a pair of "serialization fence instructions" to ensure that that modifications are observed. The Burger patent does not provide those teachings which are missing from the Benkual patent. With regard to Claims 2 and 3, the Examiner has acknowledged that "Benkual does not expressly detail that an issue unit performed the threshold determination or using counters in the threshold determination". The Examiner has cited the teachings found in Burger at Col. 5, lines 30-66. The cited teachings discuss flushing any instructions out of the pipeline after a control register modification and then re-fetching the instructions, so that the modification will be implemented or delaying instructions for a predetermined latency period to ensure that the modification will be implemented. Applicants contend that Burger does not teach that an issue unit perform the flushing and delaying, and further contend that neither flushing nor delaying obviates a determination by an issue unit based on an instruction

threshold. The Examiner again cites the passage from Benkual, at Col. 17, line 63-Col. 18, line 26 with regard to counters. As discussed above, the Benkual teachings relate to two counters (in-order and not-in-order or out-of-order) within a RIFO which count available space but do not count outstanding instructions. Even if one were to modify Benkual with Burger, one would not arrive at the claimed invention, since neither patent teaches or suggests an issue unit for determining if the number of outstanding instructions is above a threshold and for issuing a fence instruction until the number of writes is below the threshold. Since neither reference teaches the claim features, a *prima facie* case of obviousness simply has not been presented by the Examiner *(In re Wilson,* 424 F.2d 1382, 165 USPQ 494 (C.C.P.A. 1970)).

The Burger patent has been cited as the only reference against Claims 4 and 5. As noted above, Burger provides a way to ensure that modifications to the control register be implemented for all successive instructions. Applicants respectfully assert that the Burger patent does not obviate the language of Claims 4 and 5. The Examiner has stated that "Burger taught the issue means retrieving operand data from memory and forwarding and the instruction to the execution unit" *(sic).* The Examiner then concludes that,

"[a]lthough Burger does not expressly detail...that the retrieved instruction comprised opcode and target location" that Burger mentions branch instructions and addresses. Applicants first disagree that Burger teaches fetching operand data. The cited passage from Col. 3, lines 31-65 teaches that Burger fetches instructions, allocates the instructions for execution at an execution unit, and executes at the execution unit. Burger does not teach or suggest fetching operand data or target location, wherein the target location is the memory location at which the results of the instruction will be stored. Applicants believe that the Examiner is incorrectly analogizing the Burger execution unit with a target memory location. Burger does not teach or suggest retrieving operand data from memory and forwarding the operand data, op code, and a target location to a execution unit. Again, Applicants respectfully conclude that the Examiner has not made out a *prima facie* case of obviousness.

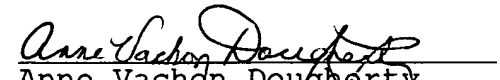
The Examiner next asserts that the remaining claims are rendered obvious by the Burger patent in view of Benkual. As argued above, the Burger patent does not teach the issue means retrieving operand data from memory and forwarding the operand data, op code, and a target location to a execution unit. Moreover, neither Burger not Benkual teaches means or

steps for issuing fence instructions designating a region of memory where no further instructions are issued until a number of writes to the designated region is below a threshold. Neither Burger nor Benkual provides for tracking the number of write instructions; neither patent provides a threshold of instructions; and, neither patent issues fence instructions for a memory region. As noted above, Benkual has a space threshold that indicates only that the RIFO is full, and Benkual counts available memory space. However, the claim language is specific to an instruction threshold and to counters which track instructions. Accordingly, Applicants conclude that the claim language is not obviated by the combination of references.

Based on the foregoing amendments and remarks, Applicants respectfully request entry of the amendments, reconsideration of the amended claim language in light of the remarks, withdrawal of the rejections, and allowance of the claims.

Respectfully submitted,

G. Bilardi, et al

By: 

Anne Vachon Dougherty
Registration No. 30,374
Tel. (914) 962-5910